Linear address:

31	24	23	16	15	8	7	0

10

10

12

page directory
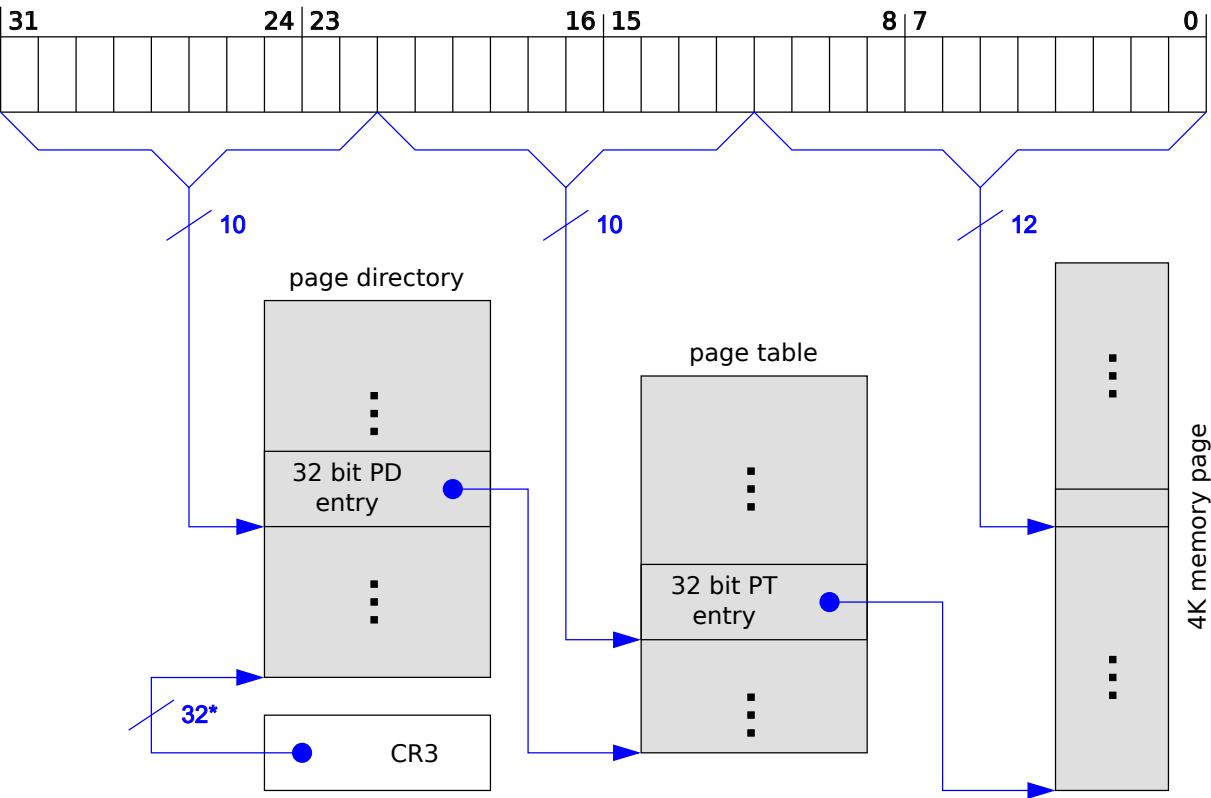
32 bit PD entry

page table

32 bit PT entry

4K memory page

32*

CR3

*) 32 bits aligned to a 4-KByte boundary